IN THE CLAIMS:

Please amend claims 1, 4, and 7 as follows:

1. (Currently Amended) A Phase-Locked Loop with multiphase clocks for use in a digital system, said Phase-Locked Loop comprising:

a main loop comprising, coupled in series, a Phase Frequency Detector, a Main Charge Pump, a Main Loop Filter, a Multi-Phase Voltage Controlled Oscillator and a Phase-switching Fractional Divider;

a calibration loop comprising Y Calibration Loop Filters, with Y being an integer, coupled to the Multi-Phase Voltage Controlled Oscillator, and Control Logic for controlling the Phase-Switching Fractional Divider; and

a ~~Multiplexer~~ Demultiplexer coupled between an output of the Main Charge Pump and inputs of the Main Loop Filter and the Y Calibration Loop Filters,

wherein ~~a Reference Frequency Signal is coupled to~~ the Phase Frequency Detector includes an input for receiving a Reference Frequency Signal,

~~a control signal from the Control Logic is coupled to~~ the ~~Multiplexer~~ Demultiplexer includes an input for receiving a control signal from the Control Logic, and

~~a Calibration Signal is coupled to a control input of~~ the Control Logic includes a control input for receiving a Calibration Signal.

2. (Original) A fractional-N frequency synthesizer comprising the Phase-Locked Loop according to claim 1.

3. (Original) An integrated circuit comprising at least one Phase-Locked Loop according to claim 1.

4. (Currently Amended) A digital mobile radio communication apparatus including at least one Phase-Locked Loop with multiphase clocks, said Phase-Locked Loop comprising:

a main loop comprising, coupled in series, a Phase Frequency Detector, a Main Charge Pump, a Main Loop Filter, a Multi-Phase Voltage Controlled Oscillator and a Phase-switching Fractional Divider;

a calibration loop comprising Y Calibration Loop Filters, with Y being an integer, coupled to the Multi-Phase Voltage Controlled Oscillator, and Control Logic for controlling the Phase-Switching Fractional Divider; and

a ~~Multiplexer~~ Demultiplexer coupled between an output of the Main Charge Pump and inputs of the Main Loop Filter and the Y Calibration Loop Filters,

wherein ~~a Reference Frequency Signal is coupled to~~ the Phase Frequency Detector includes an input for receiving a Reference Frequency Signal,

~~a control signal from the Control Logic is coupled to~~ the ~~Multiplexer~~ Demultiplexer includes an input for receiving a control signal from the Control Logic, and

~~a Calibration Signal is coupled to a control input of~~ the Control Logic includes a control input for receiving a Calibration Signal.

5. (Original) The digital mobile radio communication apparatus according to claim 4, further including at least one fractional-N frequency synthesizer that comprises said Phase-Locked Loop.

6. (Original) The digital mobile radio communication apparatus according to claim 4, further including at least one integrated circuit that comprises said Phase-Locked Loop.

7. (Currently Amended) A method for synthesizing frequencies ~~with~~ in a digital system using a Phase-Locked Loop with multiphase clocks, said method comprising the steps of:

providing at least one Phase-Locked Loop ~~that includes~~ in the digital system, the Phase-Locked Loop including:

a main loop comprising, coupled in series, a Phase Frequency Detector, a Main Charge Pump, a Main Loop Filter, a Multi-Phase Voltage Controlled Oscillator and a Phase-switching Fractional Divider;

a calibration loop comprising Y Calibration Loop Filters, with Y being an integer, coupled to the Multi-Phase Voltage Controlled Oscillator, and Control Logic for controlling the Phase-Switching Fractional Divider; and

a ~~Multiplexer~~ Demultiplexer coupled between an output of the Main Charge Pump and inputs of the Main Loop Filter and the Y Calibration Loop Filters; and

synthesizing frequencies in the digital system using the Phase-Locked Loop by applying a reference frequency signal to the Phase Frequency Detector of the Phase-Locked Loop,[;] and applying a Calibration Signal to the Control Logic of the Phase-Locked Loop.

8. (Original) The method according to claim 7, wherein a fractional-N frequency synthesizer comprises the Phase-Locked Loop.

9. (Original) The method according to claim 7, wherein an integrated circuit comprises the Phase-Locked Loop.

10. (Original) The method according to claim 7, wherein a digital mobile radio communication apparatus comprises the Phase-Locked Loop.